## REMARKS

Applicants thank the Examiner for the thorough consideration given the present application. Claims 1-20 are currently being prosecuted. The Examiner is respectfully requested to reconsider his rejections in view of the amendments and remarks as set forth below.

*Citation of References*

It is noted that the Examiner has relied on two references for the art rejection, namely, Takahashi et al. (U.S. Patent No. 5,903,239) and Stopperan (U.S. Patent No. 5,719,749). Applicants further note that neither of these references is cited on the PTO 892 attached to the current rejection. Accordingly, Applicants request that the Examiner properly cite these two references.

*Rejection under 35 USC 103*

Claims 1-20 stand rejected under 35 USC §103 as being obvious over Takahashi et al. in view of Stopperan. This rejection is respectfully traversed.

The Examiner states that Takahashi et al. shows a multi-chip integrated module having a transparent substrate 1a with a circuit layer formed on the surface of the transparent substrate including chips 52 and interconnection terminals and a plurality of electrical pads 4. The Examiner admits that Takahashi et al. does not disclose a circuit substrate which attaches to the transparent substrate including a circuit layer of the circuit substrate.

The Examiner relies on Stopperan to show a circuit substrate 40 including a circuit layer, overlay 40, where the electrical pads 36 and 68 of the transparent substrate electrically connect to the circuit layer of the circuit substrate. The Examiner feels it would have been obvious to one of ordinary skill in the art to make a circuit substrate attached to the transparent substrate of Takahashi et al. as taught by Stopperan. Applicants submit that the amended claims are not obvious over this combination of references.

It is noted that FIG. 1 of the Takahashi et al. reference shows an antenna apparatus having an antenna chip 51 and circuit chips 52. The circuit chips are mounted directly on the microstrip line 8a and microstrip line 7 by way of bumps 6a. The microstrip lines are on a dielectric film 3a which is on a ground conductor film 2a. The ground conductor is on one surface of the substrate 1a. No circuit line is directly formed on the substrate 1a. The ground connector film 2a is usually made of metal, which is not transparent.

This differs from the present invention which is a multi-chip integrated module. In this arrangement, the two chips are directly mounted on the circuit layer 111 of the transparent substrate. Since the substrate is transparent, it is possible for the chips to be easily mounted on the substrate using a CCD camera to help position the chips as they are bonded to the substrate. As a result, it is possible to attain a higher density of the circuit layer 110 and reduce the size of the package.

Referring to FIG. 2, the Stopperan reference shows a printed circuit assembly 10 including a printed circuit board 20 with a flexible printed circuit overlay 40 mounted thereto. The overlay 40 does not attach to the transparent substrate. The overlay 40 is attached to the printed circuit board 20 and the material of the printed circuit board 20 is not mentioned to be transparent.

Claim 1 as amended, points out that the circuit layer is formed directly on one surface of the transparent substrate. This is not seen in either reference. In Takahashi et al., the microstrip lines are formed on top of a dielectric film which is separated from the substrate by a ground conductor layer. As a result, it is not possible to observe the placement of the chips directly due to the non-transparent layers. Further, claim 1 describes a circuit substrate which is attached to the transparent substrate. Even if Stopperan shows overlay 40, this is not mounted on the substrate, but is instead mounted on the printed circuit board which prevents visual observation. For these reasons, Applicants submit that claim 1 is allowable over the combination of references.

Claim 13 is another independent claim which shows similar limitations to claim 1. Thus, this claim also recites the formation of the circuit layer directly on one surface of the transparent substrate. Accordingly, Applicants submit that claim 13 is also allowable for similar reasons recited above in regard to claim 1.

Claims 2-12 and 14-20 depend from these allowable independent claims and as such are also considered to be allowable. In addition, each of these claims recites other features which make them additionally allowable. For example, claim 8 describes the hollow portion of the circuit substrate which is not seen in either of the references. Accordingly, these claims are additionally allowable.

Changes to the Specification

Applicant has submitted herewith a Substitute Specification together with a marked-up copy of the original specification showing the matter being added to and deleted from the specification.

Applicant has amended the specification to specify the two different groups of bumps as first bumps and second bumps. This distinction follows directly from the original specification where the bumps function to connect to different items. This is also indicated by the different reference numerals. Accordingly, no new matter is being entered. Applicant has also amended the claims in similar fashion to distinguish between the different groups of bumps in the claims.

*Conclusion*

In view of the above amendments and remarks, it is believed that the claims clearly distinguish over the patents relied on by the Examiner, either alone or in combination. In view of this, reconsideration of the rejections and allowance of all claims are respectfully requested.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

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Respectfully submitted,

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